Amorphous-Silicon Inter-Layer Grating Couplers With Metal Mirrors Toward 3-D Interconnection

JoonHyun Kang, *Student Member, IEEE*, Yuki Atsumi, *Student Member, IEEE*, Yusuke Hayashi, *Student Member, IEEE*, Junichi Suzuki, Yuki Kuno, Tomohiro Amemiya, *Member, IEEE*, Nobuhiko Nishiyama, *Senior Member, IEEE*, and Shigehisa Arai, *Fellow, IEEE*

***Abstract*—Inter-layer grating couplers sandwiched by two metal layers were demonstrated for high coupling efficiency vertical coupling between amorphous-Si:H multi-stacked optical waveguides. A coupling efficiency of 83% was achieved with grating couplers formed on 5 μm wide waveguides separated by 1 μm while theoretical coupling efficiency of 90% was obtained.**

***Index Terms*—Silicon photonics, amorphous-Si:H (a-Si:H) waveguide, multi-layer, vertical coupler, grating coupler, metal mirror.**

I. Introduction

THE optical interconnects are considered to be a critical technology for transmitting data in next-generation high-performance LSI chips [1], [2], as it can overcome the several difficulties that conventional electrical interconnects are facing due to the limitation in bandwidth capacity of metal wires [3]. As a promising approach for implementing such optical interconnects, Si photonics has the potential benefits of providing a high degree of integration with current Si-based LSI chips in addition to the high-speed signal transmission. Optical components such as passive devices, modulators, photodetectors, and hybrid integration of lasers have been demonstrated on silicon on insulator (SOI) [4]–[7].

Photonic devices and electronic LSI chips can share the Si-based platform; however, they function best under substrate specifications that are quite different. For example, the typical buried oxide (BOX) thickness of SOI wafers is $\sim$3 μm for photonic devices compared to less than 200 nm for state-of-the-art CMOS chips. Therefore, integrating photonic devices on LSI chips by a back-end process is a possible solution since there is no need to change the structures of the CMOS circuits. This requires that the fabrication process should be completed at temperatures below 400 °C to avoid damage to the CMOS circuits. For such requirement, hydrogenated amorphous silicon (a-Si:H) can be deposited at a temperature below 300 °C by plasma-enhanced chemical-vapor-deposition (PECVD) and satisfies the back-end process compatibility, although the deposition temperature of crystalline Si is usually over 1000 °C. There have been several reports on the low-loss property of a-Si:H waveguides. Many works have focused on the passivation of dangling-bonds by H atoms in order to reduce the absorption loss of a-Si:H [8], [9]. In a recent report, a loss of 1.2 dB/cm was achieved with wet etched a-Si:H film [10].

There are additional advantages of using a-Si:H. Multi-layer stacking of a-Si:H can be easily achieved by depositing alternating layers of a-Si:H and SiO_2 films, which allows the creation of a high-density three-dimensional (3-D) optical circuit [11].

For realization of the multi-layered optical circuits, vertical coupling between the layers is necessary. Unlike in electronic connections such as VIAs [12], a vertical structure is not so easy to achieve in optical connection. Until now, mainly two types of vertical couplers have been investigated. One is a vertical coupler employing a directional coupler design [13]. High coupling efficiency is expected with such a structure; however, the distance between layers is typically limited to around 200 nm in order to achieve sufficient mode overlap. This causes undesired crosstalk in sections that should not have any coupling. Therefore, it is desired that the inter-layer distance be a relatively large value, such as 1 μm. Using the directional coupler for such separation distance, it requires multiple couplers in order to couple light between vertically displaced photonic planes with a large separation [14]. The other approach is to use a pair of grating couplers. This approach can transfer light over a long distance of more than a few micrometers [15]–[17]. We proposed to use a pair of grating couplers for the inter-layer coupling at the inter-layer distance of 1 μm and achieved the coupling efficiency of 22% in the previous report [18]. These types of grating couplers were also reported for a chip-to-chip coupling between two separate SOI chips where two grating couplers were fabricated on two separate SOI chips and coupled through the air gap [19], [20].

In this paper, we propose and demonstrate a novel inter-layer grating couplers sandwiched by metal mirrors for efficient coupling between multi-layered a-Si:H waveguides. In

Manuscript received October 4, 2013; revised December 1, 2013; accepted January 8, 2014. Date of publication January 14, 2014; date of current version March 11, 2014. This work was supported by the Ministry of Education, Culture, Sports, Science and Technology; by JSPS KAKENHI under Grants #24246061, #25709026, #21226010, #25420321, #11J08863, and #13J08096; by the Council for Science and Technology Policy under the Funding program for World-Leading Innovative R&D in Science and Technology; and by the New Energy and Industrial Technology Development Organization. The work of J. Kang and Y. Atsumi was supported by the Japan Society for the Promotion of Science for the Research Fellowship for Young Scientists.

J. Kang, Y. Atsumi, Y. Hayashi, J. Suzuki, Y. Kuno, and N. Nishiyama are with the Department of Electrical and Electronic Engineering, Tokyo Institute of Technology, Tokyo 152–8552, Japan (e-mail: kang.j.aa@m.titech.ac.jp; atsumi.y.ab@m.titech.ac.jp; hayashi.y.ao@m.titech.ac.jp; suzuki.j.af@m.titech.ac.jp; kuno.y.ad@m.titech.ac.jp; n-nishi@pe.titech.ac.jp;).

T. Amemiya and S. Arai are with the Department of Electrical and Electronic Engineering and the Quantum Nanoelectronics Research Center, Tokyo Institute of Technology, Tokyo 152–8552, Japan (e-mail: amemiya.t.ab@m.titech.ac.jp; arai@pe.titech.ac.jp).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSTQE.2014.2300058

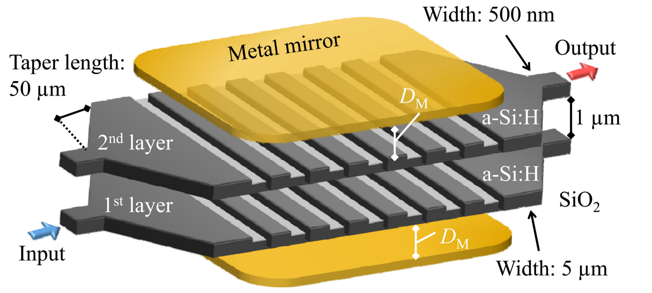

Fig. 1. Schematic image of the inter-layer grating couplers with metal mirrors.

Section II, details of the device structure and the coupling efficiency of the inter-layer grating couplers depending on the gratings and the metal mirrors will be described. Then, Section III provides the experimental results from the fabrication and the measured coupling efficiency.

II. Device Structure and Design

A schematic of the proposed inter-layer grating coupler is given in Fig. 1. Unlike the grating couplers between single-mode fibers and photonic-wire waveguides, our inter-layer couplers consist of a pair of grating couplers sandwiched between metal mirrors so as to reflect light back to the grating couplers. The inter-layer distance between each grating coupler is 1 μm in this study, which is necessary to suppress the crosstalk below -30 dB between vertically-stacked-waveguides [21], although a longer inter-layer distance is also possible as needed. For the longer inter-layer distance, an offset in the propagation direction between the multi-layered gratings is needed because the diffraction angle is typically around 10°. The details of structure parameters of the inter-layer grating couplers will be discussed in the next.

A. Device Design

The inter-layer grating couplers consist of three parts: a taper section for smooth connection between the wire waveguides and wide-width waveguides, two-layered grating couplers, and metal mirrors.

Wide-width waveguides were used at the gratings in order to expand coupling tolerance caused by fabrication errors and beam divergence angle in the orthogonal (to the waveguide propagation) direction. Conventional wire waveguides (500-nm-wide) were used for the input and the output of the inter-layer grating couplers. Between the wire and the wide-width waveguides, a 50-μm-long linear taper was used to allow only the fundamental mode to propagate into the grating region.

For the grating section, shallow etched (70-nm deep) gratings were used in order to suppress the backward reflection from the gratings instead of fully etched gratings, which were used in the previous report [18]. The calculated backward reflection was less than -23 dB at the input port. The inter-layer grating couplers were optimized by 3-D finite-difference time-domain (FDTD) simulation with 3 main parameters: grating period (Λ), the number of grating periods (N), and the distance from the gratings to the metal mirrors (D_M). The wavelength and the polarization were fixed at 1.55 μm, and only the transverse-electric mode was considered in the simulations in

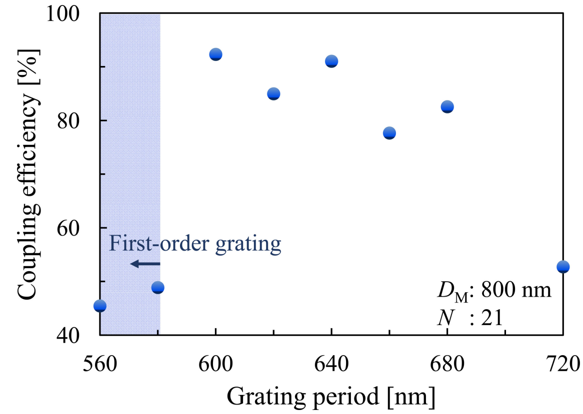

Fig. 2. Coupling efficiency as a function of the grating period (Λ).

this section. The refractive indices of a-Si:H and SiO_2 were set to be 3.48 and 1.45, respectively. Au was used as a material for the metal mirrors in this study due to our evaporation system limitation, though Al which is already established in CMOS technology is also a good candidate. The coupling efficiency with Al mirrors showed less than 1% difference compared with the value with Au mirrors. The details of the simulation results are as follows.

The coupling efficiency was calculated with various grating periods ranging from 560 to 720 nm (see Fig. 2). We used uniform gratings with the duty cycle of 50% (in physical length) in order to simplify the calculation steps. In this calculation, D_M and N were fixed to be 800 nm and 21, respectively. The coupling efficiency of 92% and 90% are obtained at Λ of 600 and 640 nm, respectively, while it decreases at Λ of 620 nm because of the mismatch in mode profile between the diffracted light and the gratings deriving from the different diffraction angle. With a longer grating period, the peak wavelength of the coupling efficiency shifts to the longer wavelength. For grating periods shorter than 580 nm, the gratings shows first-order diffraction, which leads to an increase of the backward reflection. We choose to use Λ of 640 nm instead of 600 nm, in order to avoid the backward reflection in the case of the deviation in duty cycle or the thickness of the a-Si:H layer occurred due to the fabrication errors and the actual refractive-indices were different from those of used in the simulation.

The second parameter is the number of grating periods N. The same N was used for both the first and second layer gratings. As N increases, the power transfers to the other side of the grating coupler will increase gradually and then, light will return to the original grating coupler and repeat the above behavior. Fig. 3 shows N dependence of the coupling efficiency for three different D_M. The coupling efficiency has a peak at a certain number of grating periods as mentioned before. The highest coupling efficiency was obtained when D_M and N are 800 nm and 21, respectively. The coupling efficiency for different D_M takes a peak value at a different number of grating periods due to the phase matching condition between the light diffracted from the gratings and reflected light from the metal mirrors. The coupling efficiency for different D_M takes a peak value at the different number of grating periods due to the phase-matching condition between diffracted light from the gratings

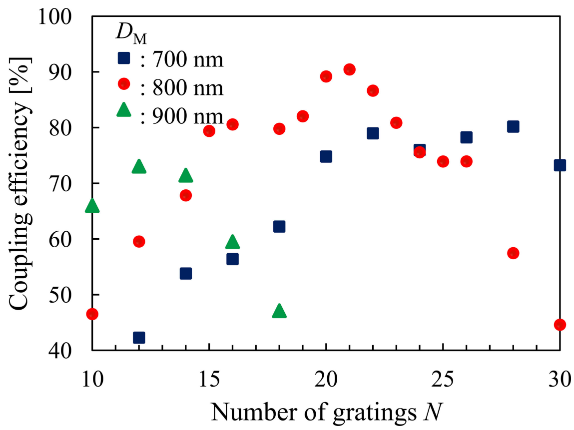

Fig. 3. Calculated coupling efficiency as a function of the number of grating periods (N) for different metal distances (D_M). Blue squares: D_M = 700 nm, red circles: D_M = 800 nm, and green triangles: D_M = 900 nm.

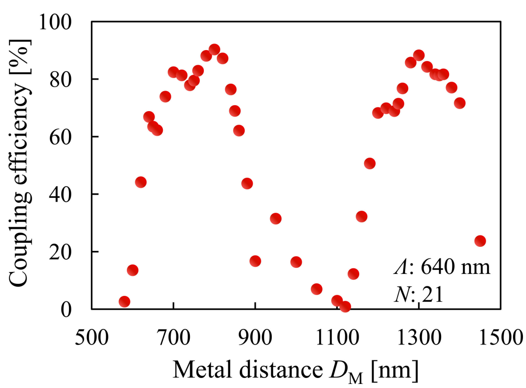

Fig. 4. Calculated coupling efficiency as a function of the metal distance (D_M).

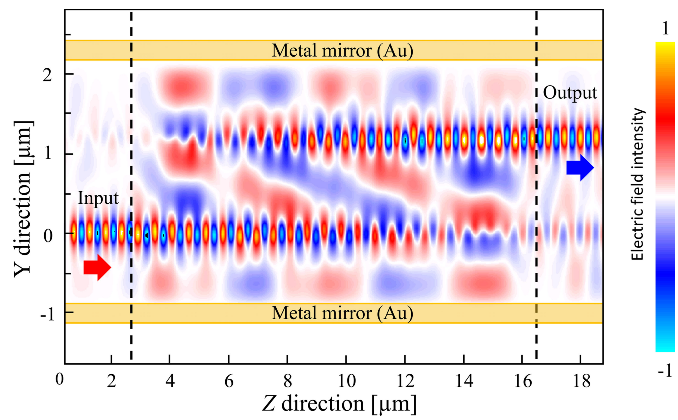

Fig. 5. Calculated electric field distribution of the inter-layer grating couplers with metal mirrors (cross-section).

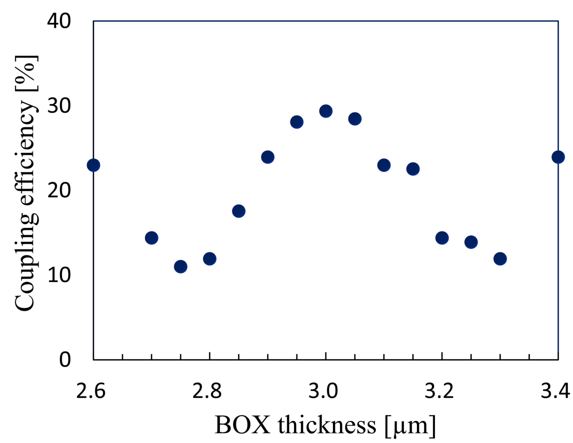

Fig. 6. Calculated coupling efficiency of inter-layer grating couplers without metal mirrors as a function of BOX thickness.

and the light reflected from the metal mirrors. Therefore, when the effective length of the light path which is determined by the D_M value and the diffraction angle of the gratings matches to the wavelength of the light, the peak coupling efficiency can be obtained. The D_M dependence of the coupling efficiency is shown in Fig. 4, where the grating period Λ and the number of the gratings N are fixed to be 640 nm and 21, respectively. The coupling efficiency shows periodic changes and takes peak values at D_M of 800 and 1300 nm. In contrast, the coupling efficiency approaches 0% when D_M is 600 or 1100 nm. Hence, D_M is the key issue to control in the inter-layer grating couplers.

Fig. 5 shows the electric-field distribution (Specifically that of E_X, which is oriented along the orthogonal direction) with the parameters of Λ: 640 nm, N: 21 and D_M: 800 nm. The light input is from the left end of the first layer waveguide and it is output from the right end of the second layer waveguide. The X, Y, and Z directions are the orthogonal, vertical, and propagation directions, respectively. Diffraction angle of the beam was 8°.

In order to confirm the contribution of the metal mirrors to the device performance, we also calculated the coupling efficiency of the inter-layer grating couplers without metal mirrors. For comparison, we used the same gratings (Λ: 640 nm, N: 21) and inter-layer distance of 1 μm. In the case without metal mirrors, we assumed that the reflection comes from the substrate under the BOX layer instead of from the metal mirrors. For the phase condition of the reflected light, we varied the BOX thickness around 3 μm which is a typical value for the photonic devices. Fig. 6 shows the coupling efficiency as a function of the BOX thickness. The maximum coupling efficiency of 30% can be obtained at the BOX thickness of 3 μm.

B. Wavelength Dependence

Fig. 7 shows the wavelength dependence of the coupling efficiency. By introducing metal mirrors, the coupling efficiency can be increased to 3 times higher value (90%) and the -1dB (coupling efficiency $> 80\%$) bandwidth becomes 80 nm (from 1520 to 1600 nm), which can cover the full C-band wavelength range.

C. Tolerance to Misalignment

Since each part of the inter-layer grating couplers will be fabricated monolithically on a single substrate, the alignment between the gratings on each layer is difficult to correct after the fabrication stage. Therefore, tolerance to misalignment is important from a practical point of view. Tolerance to misalignment in the vertical direction was already discussed in terms of the parameter D_M (the thickness of the SiO_2). Here, we will

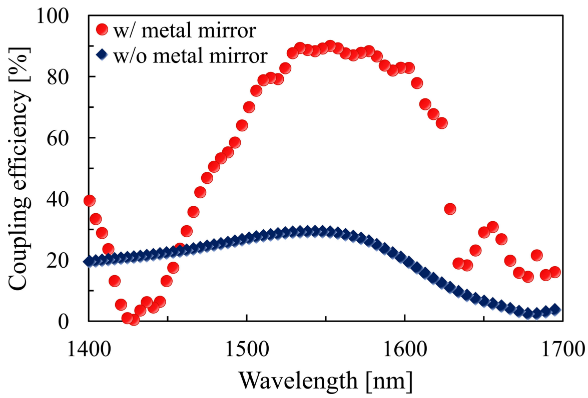

Fig. 7. Wavelength dependence coupling efficiency of inter-layer grating couplers with and without metal mirrors (Λ: 640 nm, N: 21, D_M : 800 nm).

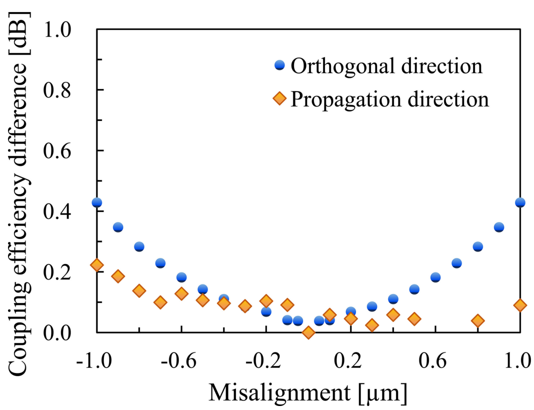

Fig. 8. Deviation of the coupling efficiency as a function of the misalignment in the propagation direction and the orthogonal (width) direction.

consider the in-plane misalignment, in both the propagation direction and the orthogonal direction. As can be seen in Fig. 8, the deviation of the coupling efficiency is below 0.5 dB even with a 1-μm misalignment for both the propagation and the orthogonal directions. In addition, the coupling tends to be more tolerant to misalignment in the propagation direction, due to the larger dimension of the gratings in that direction, which was a length of $\sim$13.5 μm compared to a width of 5-μm.

III. Fabrication and Measurement

In this section, the experimental results of the inter-layer grating couplers with metal mirrors are described.

A. Fabrication

The inter-layer grating couplers were fabricated based on the simulation results discussed in Section II (Λ: 640 nm, D_M: 800 nm, N: 18–26). All the fabrication processes were carried out at temperatures below 300 °C including deposition of a-Si:H film. A two-inch Si substrate covered with 3-μm-thick layer of thermal oxide (SiO_2) was prepared as the initial wafer. The first step was evaporation of a 100-nm-thick Au film and lift-off. Alignment marks for electron beam (EB) lithography and the bottom mirrors were formed. The Au patterns were buried by deposition of SiO_2 at the process temperature of 300 °C. Then the surface of the SiO_2 was flattened by a chemical mechanical

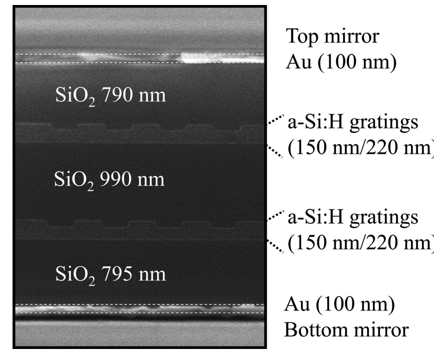

Fig. 9. Cross-sectional SEM image of the fabricated inter-layer grating couplers with metal mirrors.

polishing (CMP) process (Standard SS25 silica slurry for the first step, mixture of CMS8401/CMS8452 for the second step). The thickness of the SiO_2 was controlled to be equal the target value of 800 nm by the second deposition of SiO_2. As the core of the first layer, a 220-nm-thick layer of a-Si:H was deposited by PECVD with conditions as follows; SiH_4 flow rate: 100 sccm, Ar flow rate: 100 sccm, power: 100 W, and deposition temperature: 300 °C. Patterning was carried out by employing two steps of EB lithography for waveguides and gratings, and an inductively coupled-plasma reactive-ion-etching system. The waveguide patterns were buried by SiO_2 deposition, and the CMP process was again carried out, followed by SiO_2 deposition to the thickness of 1 μm (corresponds to the inter-layer distance). For the second layer, a 220-nm-thick a-Si:H film was deposited and patterned, as was done for the first layer. Next, SiO_2 deposition and the third CMP treatment were performed to the thickness of 800 nm. The final step is to form the upper mirrors in the same way that the bottom mirrors were formed. All thicknesses were monitored by an ellipsometry during the measurement for accurate thickness control.

Fig. 9 shows the cross-sectional SEM image of the fabricated inter-layer grating couplers. From the SEM image, the D_M values for the first and second layers were measured to be 795 and 790 nm, respectively. The deviation of the thickness was $\sim$10 nm (target thickness: 800 nm) including the inter-layer distance.

B. Measurement

For the transmission measurements, lensed-tip single-mode fibers were used for the input and output of the inter-layer grating couplers by edge coupling through inverted-taper spot-size converters [22]. From an ASE source, a range of wavelengths around 1.55 μm was used as the input. We calculated the mean value of measured transmittances within the first to the first layer and the second to the second layer which was fabricated without grating couplers, separately. Then we also measured the transmittance between the input to the first layer and the output from the second layer with the grating couplers. The coupling efficiency was calculated by subtracting the mean value from the measured transmittance of the inter-layer grating couplers.

The spectral property of the coupling efficiency of the inter-layer grating couplers with 20 gratings is shown in Fig. 10. The peak coupling efficiency of 83% was obtained at the wavelength

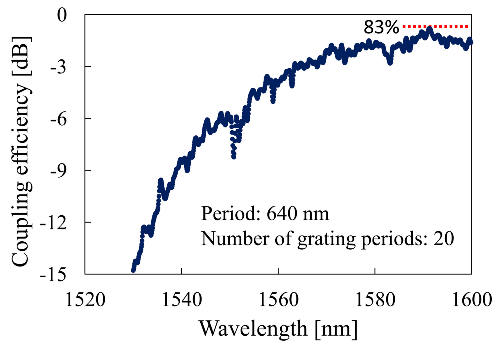

Fig. 10. Measured coupling efficiency of inter-layer grating couplers (N: 20, Λ: 640 nm, D_M : 800 nm).

of 1590 nm with $N = 20$, whereas $N = 21$ is the optimum value as described in Section II. The difference between the simulation results and measurements might come from the fabrication errors and difference in the simulation parameter as described in Section II-A. The 3-dB bandwidth was more than 40 nm, which was limited by the output wavelength range of the light source.

IV. Conclusion

In conclusion, we demonstrated inter-layer grating couplers sandwiched by metal mirrors for high efficiency coupling. A-Si:H was used as the core material for the waveguides deposited by PECVD. The device design and optimization were carefully performed using 3-D-FDTD simulations. A maximum coupling efficiency of 90% was calculated in the simulation, and an efficiency of 83% was achieved by the fabricated device. These results indicate that grating-based vertical couplers can realize very high coupling efficiency with metal mirrors and that their application to a-Si:H multi-layered optical circuits is a cost-effective way to make high-density on-chip optical interconnects.

Further improvements can be expected by introducing non-uniform gratings for higher coupling efficiency or a unique taper design between wire waveguides and gratings to attain a compact device size [23]–[25].

Acknowledgment

The authors would like to thank Prof. M. Asada, Prof. T. Mizumoto, and Prof. Y. Miyamoto, all at the Tokyo Institute of Technology, for fruitful discussions.

References

[1] K. Itoh and M. Horiguchi, "Low-voltage scaling limitations for nanoscale CMOS LSIs," *Solid-State Electron.*, vol. 53, no. 4, pp. 402–410, Apr. 2009.

[2] D. A. B. Miller, "Device requirements for optical interconnects to silicon chips," *Proc. IEEE*, vol. 97, no. 7, pp. 1166–1185, Jul. 2009.

[3] H. Fukuda, K. Yamada, T. Tsuchizawa, T. Watanabe, H. Shinojima, and S. Itabashi, "Silicon photonic circuit with polarization diversity," *Opt. Exp.*, vol. 16, no. 7, pp. 4872–4880, Mar. 2008.

[4] T. Y. Liow, K. W. Ang, Q. Fang, J. F. Song, Y. Z. Xiong, M. B. Yu, G. Q. Lo, and D. L. Kwong, "Silicon modulators and germanium photodetectors on SOI: Monolithic integration, compatibility, and performance optimization," *IEEE J. Sel. Top. Quantum. Electron.*, vol. 16, no. 1, pp. 307–315, Jan./Feb. 2010.

[5] Y. Atsumi, M. Oda, J. Kang, N. Nishiyama, and S. Arai, "Athermal wavelength filters toward optical interconnection to LSIs," *Inst. Electr., Inf. Commun. Eng. Trans.*, vol. E95-C, no. 2, pp. 229–236, Feb. 2012.

[6] Z. Zhou, Z. Tu, B. Yin, W. Tan, L. Yu, H. Yi, and X. Wang, "Development tends in silicon photonics," *Chin. Opt. Lett.*, vol. 11, no. 1, pp. 012501-1–012501-6, Jan. 2013.

[7] Y. Hayashi, R. Osabe, K. Fukuda, Y. Atsumi, J. Kang, N. Nishiyama, and S. Arai, "Low threshold current density operation of a GaInAsP/Si hybrid laser prepared by low-temperature N_2 plasma activated bonding," *Jpn. J. Appl. Phys.*, vol. 52, no. 6, pp. 060202-1–060202-3, Jun. 2013.

[8] A. Harke, M. Krause, and J. Mueller, "Low-loss singlemode amorphous silicon waveguides," *Electron. Lett.*, vol. 41, no. 25, pp. 1377–1379, Dec. 2005.

[9] S. K. Selvaraja, E. Sleeckx, M. Schaekers, W. Bogaerts, D. V. Thourhout, P. Dumon, and R. Baets, "Low-loss amorphous silicon-on-insulator technology for photonic integrated circuitry," *Opt. Commun.*, vol. 282, no. 9, pp. 1767–1770, May 2009.

[10] K. Furuya, K. Nakanishi, R. Takei, E. Omoda, M. Suzuki, M. Okano, T. Kamei, M. Mori, and Y. Sakakibara, "Nanometer-scale thickness control of amorphous silicon using isotropic wet-etching and low loss wire waveguide fabrication with the etched material," *Appl. Phys. Lett.*, vol. 100, no. 25, pp. 251108-1–251108-3, Jun. 2012.

[11] J. Kang, Y. Atsumi, M. Oda, T. Amemiya, N. Nishiyama, and S. Arai, "Low-loss amorphous silicon multilayer waveguides vertically stacked on silicon-on-insulator substrate," *Jpn. J. Appl. Phys.*, vol. 50, no. 12, pp. 120208-1–120208-3, Nov. 2011.

[12] M. Motoyoshi, "Through-silicon via," *Proc. IEEE*, vol. 97, no. 1, pp. 43–48, Jan. 2009.

[13] R. Sun, M. Beals, A. Pomerene, J. Cheng, C. Hong, L. Kimerling, and J. Michel, "Impedance matching vertical optical waveguide couplers for dense high index contrast circuits," *Opt. Exp.*, vol. 16, no. 16, pp. 11682–11690, Jul. 2008.

[14] J. T. Bessette and D. Ahn, "Vertically stacked microring waveguides for coupling between multiple photonic planes," *Opt. Exp.*, vol. 21, no. 11, pp. 13580–13591, May 2013.

[15] D. Taillaert, F. V. Laere, M. Ayre, and W. Bogaerts, "Grating couplers for coupling between optical fibers and nanophotonic waveguides," *Jpn. J. Appl. Phys.*, vol. 45, no. 8A, pp. 6071–6077, Aug. 2006.

[16] J. Feng and Z. Zhou, "Polarization beam splitter using a binary blazed grating coupler," *Opt. Lett.*, vol. 32, no. 12, pp. 1662–1664, 2007.

[17] Z. Zhou and L. Yu, "Silicon photonic devices based on binary blazed gratings," *Opt. Eng.*, vol. 52, no. 9, pp. 091708-1–091708-10, Feb. 2013.

[18] J. Kang, Y. Atsumi, M. Oda, T. Amemiya, N. Nishiyama, and S. Arai, "Layer-to-layer grating coupler based on hydrogenated amorphous silicon for three-dimensional optical circuits," *Jpn. J. Appl. Phys.*, vol. 51, no. 12, pp. 120203-1–120203-3, Nov. 2012.

[19] J. Yao, X. Zheng, G. Li, I. Shubin, H. Thacker, Y. Luo, K. Raj, J. E. Cunningham, and A. V. Krishnamoorthy, "Grating-coupler based low-loss optical interlayer coupling," in *Proc. 8th IEEE Int. Conf. Group IV Photon.*, Sep. 2011, pp. 383–385.

[20] J. Yao, I. Shubin, X. Zheng, G. Li, Y. Luo, H. Thacker, J. Lee, J. Bickford, K. Raj, J. Cunningham, and A. Krishnamoorthy, "Low loss optical interlayer coupling using reflector-enhanced grating couplers," in *Proc. 2nd Int. Conf. Opt. Interconnects Conf.*, May 2013, pp. 31–32.

[21] J. Kang, N. Nishiyama, Y. Atsumi, T. Amemiya, and S. Arai, "Multi-stacked silicon wire waveguides and couplers toward 3-D optical interconnects," in *Proc. SPIE Optoelectronic Interconnects XIII 8630*, Feb. 2013, pp. 863008-1–860308-12.

[22] H. Yamada, T. Chu, S. Ishida, and Y. Arakawa, "Si photonic wire waveguide devices," *IEEE J. Sel. Top. Quantum Electron.*, vol. 12, no. 6, pp. 1371–1379, Nov./Dec. 2006.

[23] F. Van Laere, T. Claes, J. Schrauwen, S. Scheerlinck, W. Bogaerts, D. Taillaert, L. O'Faolain, D. Van Thourhout, and R. Baets, "Compact focusing grating couplers for silicon-on-insulator integrated circuits," *IEEE Photon. Technol. Lett.*, vol. 19, no. 23, pp. 1919–1921, Dec. 2007.

[24] L. Liu, M. Pu, K. Yvind, and J. M. Hvam, "High-efficiency, large-bandwidth silicon-on-insulator grating coupler based on a fully-etched photonic crystal structure," *Appl. Phys. Lett.*, vol. 96, no. 5, pp. 051126-1–051126-3, Feb. 2010.

[25] Y. Ding, H. Ou, and C. Peucheret, "Ultrahigh-efficiency apodized grating coupler using fully etched photonic crystals," *Opt. Lett.*, vol. 38, no. 15, pp. 2732–2734, Aug. 2013.

JoonHyun Kang (S'12) was born in Seoul, Korea, in 1986. He received the B.E. and M.E. degrees in electrical and electronic engineering from the Tokyo Institute of Technology, Tokyo, Japan, in 2010 and 2012, respectively. He is currently working toward the Ph.D. degree in the Department of Electrical and Electronic Engineering, Tokyo Institute of Technology. Since 2013, he has also been working as a Research Fellow in the Japan Society for the Promotion of Science. His current research interests include 3-D a-Si:H optical circuits. Mr. Kang is a Member of the IEEE Photonics Society, the Institute of Electronics, Information and Communication Engineers, and the Japan Society of Applied Physics

Yuki Atsumi (S'09) was born in Aichi Prefecture, Japan, in 1986. He received the B.E. and M.E. degrees in electrical and electronic engineering from the Tokyo Institute of Technology, Tokyo, Japan, in 2009 and 2011, respectively. He is currently working toward the Ph.D. degree in the Department of Electrical and Electronic Engineering, Tokyo Institute of Technology. Since 2011, he has also been working as a Research Fellow in the Japan Society for the Promotion of Science. His current research interests include athermal photonic integrated devices on a silicon platform. Mr. Atsumi is a Member of the Japan Society of Applied Physics.

Yusuke Hayashi (S'12) was born in Nagano Prefecture, Japan, in 1989. He received the B.E. degree in electrical and electronic engineering from the Tokyo Institute of Technology, Tokyo, Japan, in 2012. He is currently working toward the M.E. degree in the Department of Electrical and Electronic Engineering, Tokyo Institute of Technology.His current research interests include III–V/Si hybrid photonic integrated circuits. Mr. Hayashi is a Member of the Japan Society of Applied Physics.

Junichi Suzuki was born in Kanagawa Prefecture, Japan, in 1990. He received the B.E. degree in electrical and electronic engineering from Tokyo Institute of Technology, Tokyo, Japan, in 2012. He is currently working toward the M.E. degree in the Department of Electrical and Electronic Engineering, Tokyo Institute of Technology. His current research interests include hybrid photonic integrated circuits. Mr. Suzuki is a Member of the Japan Society of Applied Physics.

Yuki Kuno was born in Ibaraki Prefecture, Japan, in 1991. He is currently working toward the B.E. degree in the Department of Electrical and Electronic Engineering, Tokyo Institute of Technology, Tokyo, Japan. His current research interests include 3-D a-Si optical circuits.

Tomohiro Amemiya (S'06–M'09) received the B.S. and Ph.D. degrees in electronic engineering from the University of Tokyo, Tokyo, Japan, in 2004 and 2009, respectively. In 2009, he moved to the Quantum Electronics Research Center, Tokyo Institute of Technology, where he is currently an Assistant Professor. His research interests are in the physics of semiconductor light-controlling devices, metamaterials for optical frequencies, magneto-optical devices, and the technologies for fabricating these devices. Dr. Amemiya is a Member of the Optical Society of America, the American Physical Society, and the Japan Society of Applied Physics. He was the recipient of the 2007 IEEE Photonics Society Annual Student Paper Award, the 2008 IEEE Photonics Society Graduate Student Fellowship, and the 2012 Konica Minolta Imaging Award.

Nobuhiko Nishiyama (M'01–SM'07) was born in Yamaguchi Prefecture, Japan, in 1974. He received the B.E., M.E., and Ph.D. degrees from the Tokyo Institute of Technology, Tokyo, Japan, in 1997, 1999, and 2001, respectively. During his Ph.D. work, he demonstrated single-mode 0.98- and 1.1-μm VCSEL arrays with stable polarization using misoriented substrates for high-speed optical networks as well as MOCVD-grown GaInNAs VCSELs. He joined Corning Incorporated, Corning, NY, USA, in 2001, and worked with the Semiconductor Technology Research Group. At Corning Incorporated, he worked on several topics, including short-wavelength lasers, 1060-nm DFB/DBR lasers, and long-wavelength InP-based VCSELs, demonstrating state-of-the-art results such as 10-Gbit/s isolator-free operation and high-temperature operation of long-wavelength VCSELs. Since 2006, he has been an Associate Professor at the Tokyo Institute of Technology. Currently, his main interests are focused on laser transistors, silicon photonics, III–V silicon hybrid optical devices, and THz-optical signal conversions involving optics–electronics–radio integration circuits. Dr. Nishiyama is a Member of the Japan Society of Applied Physics, the Institute of Electronics, Information and Communication Engineers (IEICE), and the IEEE Photonics Society. He received an Excellent Paper Award from the IEICE of Japan in 2001 and the Young Scientists' Prize in the Commendation for Science and Technology from the Minister of Education, Culture, Sports, Science and Technology in 2009.

Shigehisa Arai (M'83–SM'06–F'10) was born in Kanagawa Prefecture, Japan, in 1953. He received the B.E., M.E., and D.E. degrees in electronics from the Tokyo Institute of Technology, Tokyo, Japan, in 1977, 1979, and 1982, respectively. During his Ph.D. work, he demonstrated the room-temperature continuous wave operation of 1.11–1.67-μm long-wavelength lasers fabricated by liquid-phase epitaxy as well as their single-mode operation under a rapid direct modulation. He joined the Department of Physical Electronics, Tokyo Institute of Technology, as a Research Associate in 1982 and joined AT&T Bell Laboratories, Holmdel, NJ, USA, as a Visiting Researcher from 1983 to 1984 on leave from the Tokyo Institute of Technology. He then became a Lecturer in 1984, an Associate Professor in 1987, and a Professor with the Research Center for Quantum Effect Electronics and Department of Electrical and Electronic Engineering in 1994. Since 2004, he has been a Professor with the Quantum Nanoelectronics Research Center (QNERC), Tokyo Institute of Technology. His research interests include photonic integrated devices such as dynamic single-mode and wavelength-tunable semiconductor lasers, semiconductor optical amplifiers, and optical switches/modulators. His current research interests include studies on low-damage and cost-effective processing technologies of ultrafine structures for high-performance lasers and photonic integrated circuits on silicon platforms. Dr. Arai is a Member of the Institute of Electronics, Information and Communication Engineers (IEICE), the Optical Society of America, and the Japan Society of Applied Physics. He received an Excellent Paper Award from the IEICE of Japan in 1988, the Michael Lunn Memorial Award from the Conference on Indium Phosphide and Related Materials in 2000, Prizes for Science and Technology including a Commendation for Science and Technology from the Minister of Education, Culture, Sports, Science and Technology in 2008, and an Electronics Society Award and an Achievement Award from the IEICE, in 2008 and 2011, respectively.